# A W-band Monolithic 175-mW Power Amplifier*

H. Wang, Y. Hwang, T. H. Chen**, M. Biedenbender, D. C. Streit,
D. C. W. Lo, G. S. Dow, and B. R. Allen

TRW
Electronic Systems and Technology Division
M5/1041, One Space Park, Redondo Beach, CA 90278
TEL: (310) 814-5708 FAX: (310) 813-9623



## ABSTRACT

A monolithic W-band power amplifier has been developed to promote the output power performance. This monolithic two-stage balanced power amplifier has demonstrated a small signal gain of 7 dB and an output power of 175 mW at 90 GHz, which represents state-of-the-art output power performance for a monolithic amplifier at this frequency. This monolithic chip is fabricated using 0.1-μm AlGaAs/InGaAs/GaAs pseudomorphic power HEMT MMIC production process.

## I. INTRODUCTION

W-band power amplifier (PA) is important component in the transmitters of various W-band systems. Owing to the maturity of 0.1-μm AlGaAs/InGaAs/GaAs pseudomorphic (PM) T-gate power HEMT MMIC technology, W-band monolithic PAs with output power around 100 mW have been reported recent years [1]-[4]. Chen *et al* reported the first 100-mW PA [1] which is fabricated in R&D laboratory at TRW using unpassivated HEMTs. The 0.1-μm PM T-gate HEMT MMIC process has been successfully transferred to our production line and consolidated for the low noise and power performance in the same HEMT profile [2]. This process demonstrated good performance and high yield on both W-band MMIC low noise amplifiers (LNAs) and PAs. A monolithic balanced PA [3] and a monolithic push-pull PA [4] in W-band have been developed based on this HEMT MMIC process, respectively, with good results.

Due to the high loss for off-chip power combining at millimeter-wave (MMW) frequencies, it is desirable to obtain higher power out of single chip. This paper presents the development to promote the output power performance of a monolithic PA at W-band using 0.1-μm AlGaAs/InGaAs/GaAs pseudomorphic T-gate power HEMT MMIC production process. This two-stage balanced PA has a measured output power of 175 mW at 3-dB compression with a small signal gain of 7 dB at 90 GHz, which represents state-of-the-art output power performance for a monolithic amplifier at this frequency. It is noted that the HEMT devices used in the monolithic PA are passivated by $Si_3N_4$ for reliability concern, without much degradation of the performance.

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**T. H. Chen was with Electronic Systems and Technology Division, TRW Inc. He is now with Hexawave Photonic Systems Inc., 2 Prosperity Road II, Hsinchu, Taiwan, R. O. C.

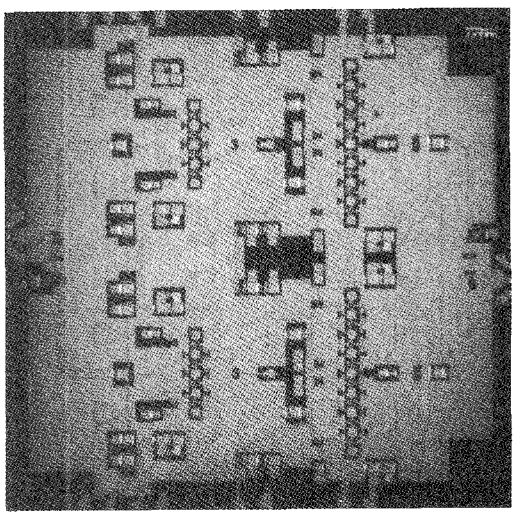
## II. DEVICE CHARACTERISTICS AND MODELING

The W-Band HEMT structure is grown using molecular beam epitaxy (MBE) on three-inch substrates and uses a PM $In_{0.22}Ga_{0.78}As$ channel. The HEMT device structure is based on a double heterostructure design to achieve a high aspect ratio for 0.1-μm gate lengths. The 0.1-μm W-band HEMT fabrication sequence shares many of the same process steps as the 0.2-μm gate length low noise and 0.15-μm gate length power HEMT production MMIC processes, ensuring high producibility [2]. The devices are passivated with PECVD silicon nitride for good reliability and robustness. Extensive characterization and statistical process control are employed for material analysis, electron beam lithography, metal-insulator-metal (MIM) dielectric thickness and capacitance, metal thickness, linewidth, and resistivity, and dc and RF device electrical parameters. This device typically exhibits a gate-to-drain breakdown voltage of 6 V measured at a gate current of 0.1 mA/mm, a peak dc transconductance of 600 mS/mm, a maximum current of 600 mA/mm, a unit current gain frequency $f_T$ of 110 GHz, and a maximum oscillation frequency $f_{max}$ of greater than 250 GHz at 2-V drain bias.

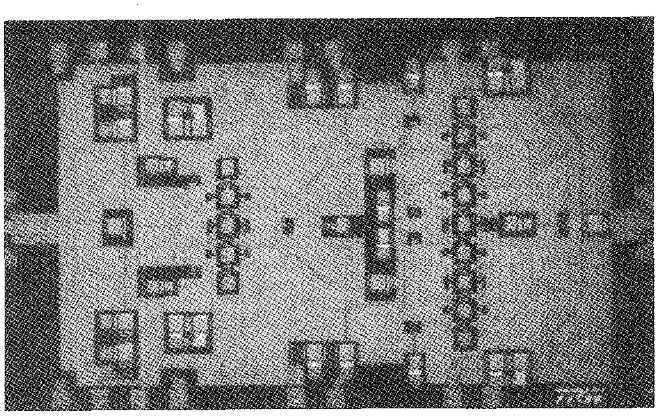
The HEMT linear small signal equivalent circuit parameters are obtained from careful fit of the measured small signal $S$-parameters to 50 GHz. These parameters are consistent with an estimation based on device physical dimensions and parameters. The Curtice-Ettenberg FET asymmetric model was used to describe the HEMT device nonlinear behavior. The nonlinear transconductance coefficients were then obtained from fitting the dc-IV measurement of the devices.

## III. CIRCUIT DESIGN

Fig. 1 (a) shows the the chip photograph of the monolithic balanced PA. The half of this balanced PA (a single-ended two-stage PA) shown in Fig. 1(b) is also fabricated on the same wafer for diagnosis purpose. The chip sizes are $4.0 \times 4.0$ mm$^2$ and $3.5 \times 2.0$ mm$^2$, respectively. The single-ended PA is a two-stage design with the first stage using a 320-µm HEMT to drive a 640-µm in the second stage. The total output gate-width is, therefore, 1280 µm for the balanced amplifier. The basic HEMT unit is a four gate-finger device with a total gate-width of 80 µm in common source configuration. Multiple reactive ion etched (RIE) via holes are employed to parallelly connect the HEMT devices in each stage for high output power.



(a)



(b)

Fig. 1. The photograph of the W-band monolithic (a) balanced, (b) single-ended, PA.

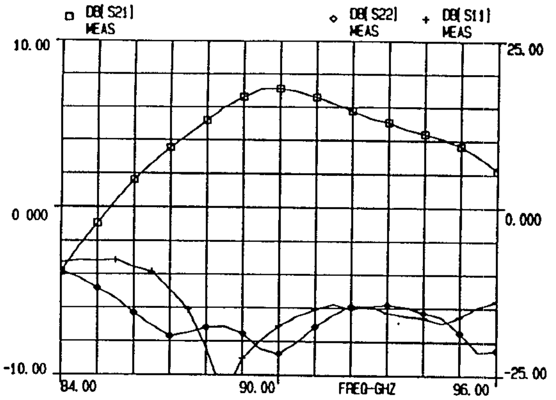
The circuit is designed for high output power based on reactive matching technique. The matching networks are comprised by cascade high-low impedance microstrip lines and open stubs on 100-µm thick GaAs substrate. MIM capacitors are used for dc block and radial stubs are employed for RF by pass. Shunt RC network are used to ensure bias network low frequency stability. Owing to high transconductance of a large total periphery, isolation resistors are placed between HEMT devices to prevent oscillation. A small resistor is also put in front of a shunt quarter-wave short stub in input matching network to help the out-of-band stability. Two identical 90° Lange couplers are used to form balanced amplifier.

A design procedure using full-wave EM analysis for the passive structures to eliminate the uncertainties due to quasi-static models was incorporated with this W-band monolithic PA design. The design methodology was described in [5]. During the circuit design, extensive EM analyses of matching structures have been performed.

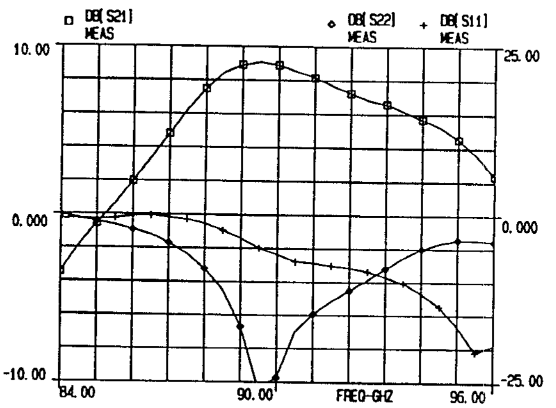
## III. MEASUREMENT RESULTS

The PA was first tested for gain via on-wafer measurement. A measured typical small signal gain of 7 dB is achieved at 90 GHz at 4-V drain voltage with gate voltage set to 0 V as shown in Fig. 2(a). Both the input and output return losses are better than 10 dB owing to the balanced design using Lange couplers. The half of the balanced amplifier is also measured. It shows a typical measured small signal gain of 9-dB at 90 GHz with higher return losses as plotted in Fig. 2(b). The PA chip was then tested in a WR-10 waveguide test-fixture for output power performance under the same bias conditions. The output power ($P_{out}$) and power added efficiency (PAE) vs. input power ($P_{in}$) curves are shown in Fig. 3. It demonstrates 22.5-dBm (175-mW) output power with about 4-dB saturated power gain at 90 GHz. The PAE is about 4% at output saturation. To our knowledge, this is the highest output power ever achieved for a single chip PA at this frequency. It is noted that this chip is developed by using standard TRW 4-mil GaAs substrate HEMT MMIC production line process. With more advanced technologies such as 2-mil substrate, compact device layout, smaller RIE via holes, or InP-based HEMTs, better results are expected.

A sampling of 24 sites of this PA (including both the single-ended and balanced PA) over three wafers have been tested for small signal gain performance. The small signal gain histograms for these circuits are plotted in Fig. 4. By using 6 dB and 8 dB for the screen criterion of the balanced and single-ended PAs, we have obtained the yield




(a)




(b)

Fig. 2. The measured small signal gain and return losses plot vs. frequency of the W-band monolithic (a) balanced, (b) single-ended, power amplifier.

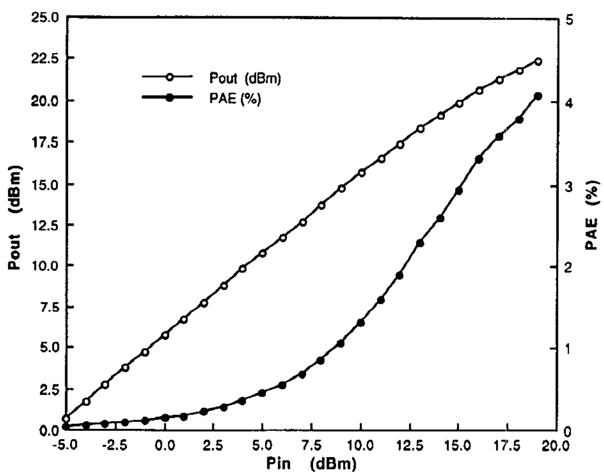



Fig. 3. The $P_{out}$ and PAE vs. $P_{in}$ plots at 90 GHz of the W-band monolithic balanced power amplifier.

numbers of 67% (16 out of 24) and 79% (19 out of 24), respectively. Good uniformity from wafer to wafer is also observed. This good yield numbers indicate the maturity of 0.1-μm power HEMT MMIC technology and the readiness of the MMIC insertion into various W-band systems with high reliability and low cost.

## IV. SUMMARY

We have presented a monolithic W-band balanced two-stage power amplifier using 0.1-μm AlGaAs/InGaAs/GaAs PM power HEMT MMIC production process technology. Measurement results show that a small signal gain of 9 dB, an output power of 175 mW, and a PAE of 4% have been achieved at 90 GHz, which represent state-of-the-art power performance of the a monolithic PA at this frequency. The success of this W-band monolithic PA indicates the maturity of power HEMT MMIC technology and the readiness of the MMIC insertion into W-band systems with high reliability and low cost.

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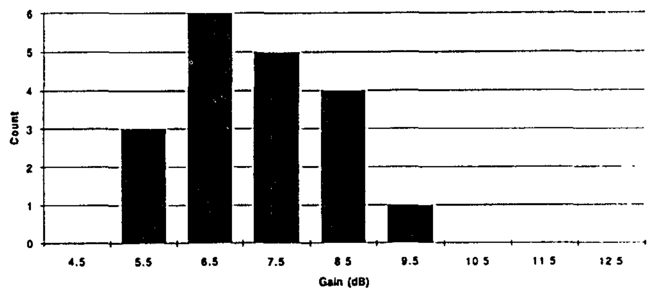
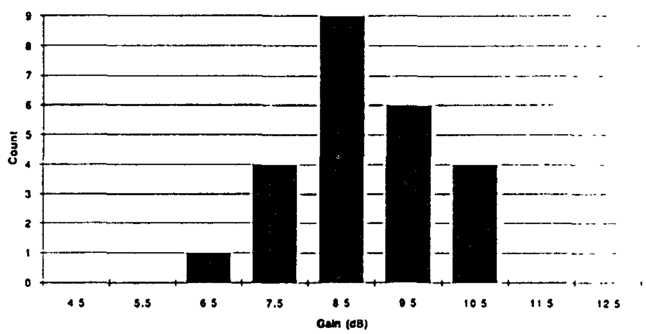



(a)




(b)

Fig. 4. The small signal gain histograms of the 24 W-band monolithic (a) balanced, (b) single-ended, PA circuits over three wafers.